The University of Jordan
King Abdullah II School for Information Technology
Computer Science Department
CS 322 Computer Organizations – Quiz#2

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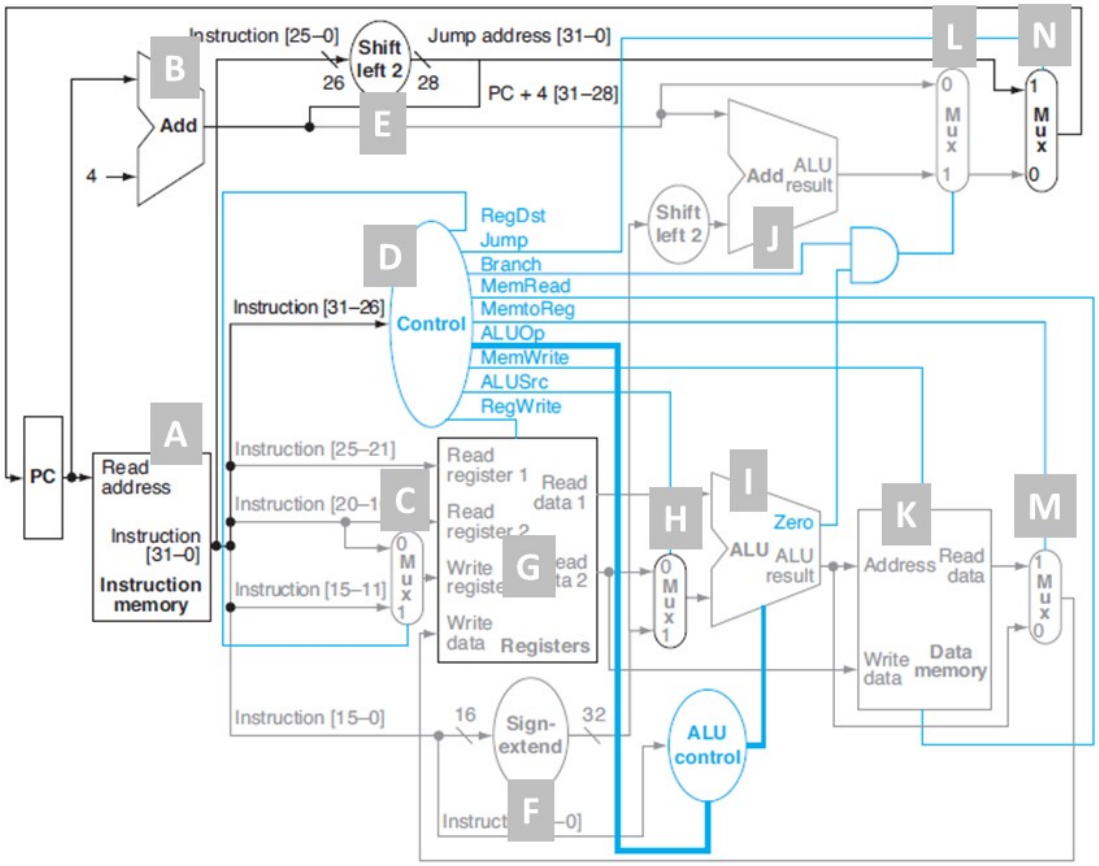
Q1 (2 Points) Consider the following simplified MIPS datapath



Referring to the labels A through N in the datapath diagram above

a) which components are **required** during the execution of a **lw** instruction?

A, C, D, F, G, H, I, K, M

b) which components are **required** during the execution of a **beq** instruction

A, D, F, G, H, I, J, L, N

Q2 (6 points) Suppose that the processor you are using has a manufacturing defect that produces a signal that is always 0 or always 1 regardless of the instruction that is being carried out. For example, **MemWrite** signal is always stuck on 0 or 1 no matter what instruction that is being executed.

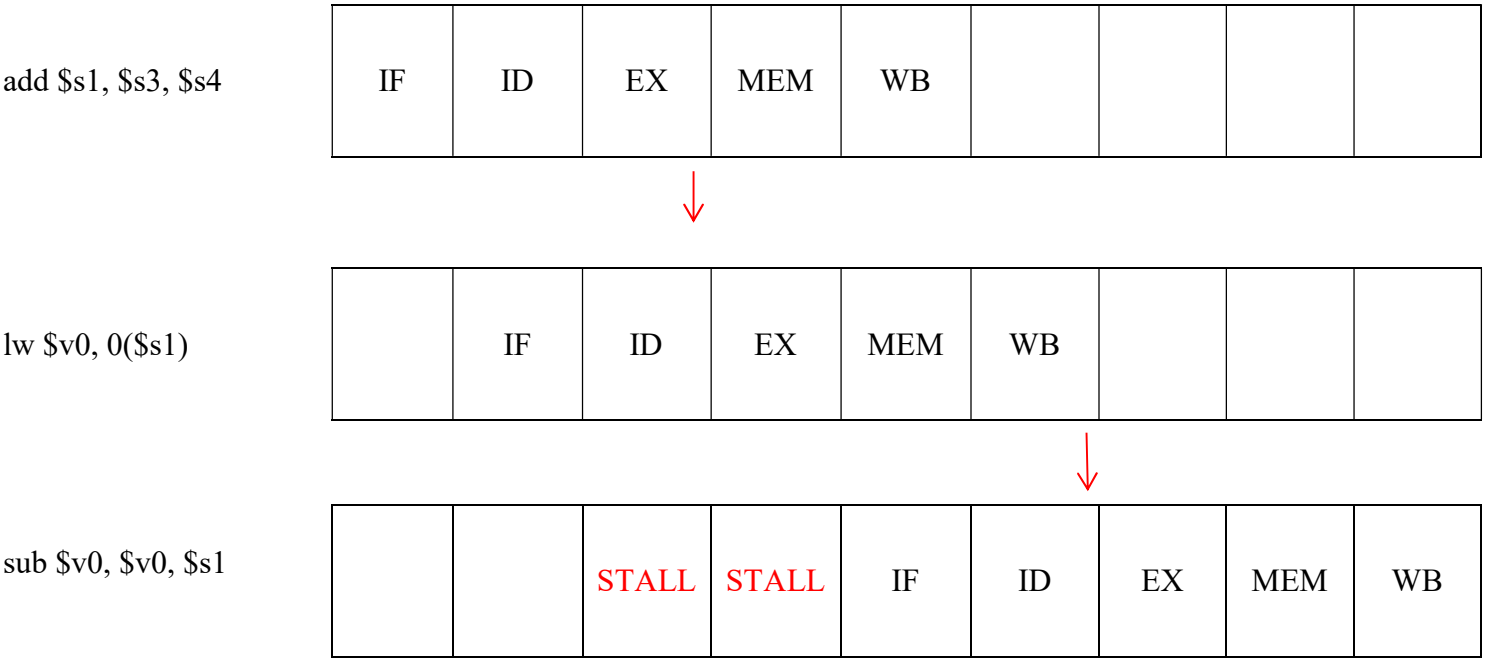
a) Assume that:
- PC = 5000
- $s0 = 0
- Memory location referenced by 0($s1) has a value: 100
- MemWrite is stuck on 1
- and we are executing **lw $s0, 0($s1)**

What are the new values of? (If the answer cannot be determined write **Unknown**)
PC = **5004**
$s0 = **0**
Memory location referenced by 0($s1) = **0**

b) Assume that:
- PC = 5000
- $s0 = 1000
- $s1 = 1500
- $s2 = 2000
- MemWrite is stuck on 1
- and we are executing **add $s0, $s1, $s2**

What are the new values of? (If the answer cannot be determined write **Unknown**)
PC = **5004**
$s0 = **3500**
$s1 = **1500**
$s2 = **2000**
Address of memory location referenced = **Unknown** and the value assigned = **Unknown**

Q3(5 Points) Draw a pipeline diagram for this code, assuming the MIPS pipeline we used in class. Show stalls and/or forwarding where needed



If you had stalls in the above code, could you re-write it to avoid the stalls?

No